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EXAMINER	
AUVE, GLENN ALLEN	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,218	KUMAR, SAMPATH HOSAHALLY	
	Examiner	Art Unit	
	Glenn A. Auve	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-33 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-33 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 22 July 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-11, and 27-31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 is rejected based on lack of positive antecedent basis of "the interrupt signal" on line 3 and "the expansion bus" on lines 3-4.

Claims 2-7 are rejected because they depend on claim 1.

Claim 8 is rejected based on lack of positive antecedent basis of "the bus" on line 7.

Claims 9-11 are rejected because they depend on claim 8.

Claim 27 is rejected based on lack of positive antecedent basis of "the interrupt signal" on line 4.

Claim 28 is rejected based on lack of positive antecedent basis of "the interrupt signal" on line 3.

Claim 30 is rejected because it is an apparatus claim, however it recites what appears to be a method step in the last line of the claim. Therefore it is unclear which statutory class of invention applicant is attempting to claim.

Claims 27,29, and 31 are rejected based on lack of positive antecedent basis of "the machine" on line 2. While the claims recite an article of machine-readable media, there is no machine positively recited.

Claim Objections

3. Claim 20 is objected to because of the following informalities: in claim 20, line 1, "on" should be "one". Appropriate correction is required.

4. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the specification does not provide any antecedent for an article of machine-readable media as recited in claims 27,29, and 31.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1,2,7,12-15,22-28,31, and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by Williams et al., U.S. Pat. No. 6,665,750 B1.

As per claim 1, Williams shows a method of processing interrupts, the method comprising: detecting an indicator of an interrupt from a expansion device(fig.2,(54)); transferring data related to the interrupt signal from the device across the expansion bus to a local memory (58); and processing the data related to the interrupt (64). Williams shows all of the elements recited in claim 1.

As for claim 2, the argument for claim 1 applies. Williams also shows detecting an indicator of an interrupt further comprising receiving an interrupt at a central processor (62). Williams shows all of the elements recited in claim 2.

As for claim 7, the argument for claim 1 applies. Williams also shows transferring data further comprising updating a memory access monitor bit in a memory access monitor status register (56,58). Williams shows all of the elements recited in claim 7.

As per claim 12, Williams shows a method of processing interrupts, the method comprising: detecting an update to a descriptor memory (54); updating a register corresponding to the descriptor memory in a local status register (56); generating an interrupt to a central processor (60); identifying a device generating the update (62); and performing a task associated with the descriptor memory (fig.2 or 3, abstract and cols. 4-5). Williams shows all of the elements recited in claim 12.

As for claim 13, the argument for claim 12 applies. Williams also shows detecting an update to a descriptor memory further comprising detecting an update to a descriptor memory using a memory access monitor (fig.2 or 3, abstract and cols. 4-5). Williams shows all of the elements recited in claim 13.

As for claim 14, the argument for claim 12 applies. Williams also shows performing a task further comprising transmitting a packet (fig.2 or 3, abstract and cols. 4-5). Williams shows all of the elements recited in claim 14.

As for claim 15, the argument for claim 12 applies. Williams also shows that performing a task further comprises determining a next hop for a received packet (cols. 4-5, wherein the device is a network device with a media access controller, and the device receives and transmits data between the system and the network). Williams shows all of the elements recited in claim 15.

As per claim 22, Williams shows a device, comprising: a central processor having at least one direct memory access controller (12); an expansion bus (20); at least one expansion device (18) in communication with the central processor through the expansion bus; and a memory access monitor electrically coupled to a memory to detect updates to the memory made by an expansion device (14). Williams shows all of the elements recited in claim 22.

As for claim 23, the argument for claim 22 applies. Williams also shows the memory access monitor further to detect an update to a receive descriptor memory (fig.2 or 3, abstract and cols. 4-5). Williams shows all of the elements recited in claim 22.

As for claim 24, the argument for claim 22 applies. Williams also shows the memory access monitor further to detect an update to a transmission descriptor memory (fig.2 or 3, abstract and cols. 4-5). Williams shows all of the elements recited in claim 24.

As for claim 25, the argument for claim 22 applies. Williams also shows the memory access monitor being implemented inside a system controller (14). Williams shows all of the elements recited in claim 25.

As for claim 26, the argument for claim 22 applies. Williams also shows the memory access monitor being implemented in software executed by a system controller (fig.2 or 3, abstract and cols. 4-5). Williams shows all of the elements recited in claim 26.

As per claim 27, Williams shows an article of machine-readable media, the article containing instructions that when executed cause the machine to: detect an indicator of an interrupt from a expansion device; transfer data related to the interrupt signal from the device across an expansion bus to a local memory; and process the data related to the interrupt from the local memory (fig.2 or 3, abstract and cols. 4-5). Williams shows all of the elements recited in claim 27.

As per claim 28, Williams shows a device, comprising: means for detecting an interrupt indicator from a expansion device; means for transferring data related to the interrupt signal from the device to a local memory; and means for processing the data related to the interrupt (fig.2 or 3, abstract and cols. 4-5). Williams shows all of the elements recited in claim 28.

As per claim 31, Williams shows an article of machine-readable media, the article containing instructions that when executed cause the machine to: detect an update to a descriptor memory; update a register corresponding to the descriptor memory in a local status register; generate an interrupt to a central processor; identify a device generating the update; and perform a task associated with the descriptor memory (fig.2 or 3, abstract and cols. 4-5). Williams shows all of the elements recited in claim 31.

As per claim 32, Williams shows a device, comprising: means for detecting an update to a descriptor memory; means for updating a register corresponding to the descriptor memory in a local status register; means for interrupting a central processor; means for identifying a device generating the update; and means for performing a task associated with the update (fig.2 or 3, abstract and cols. 4-5). Williams shows all of the elements recited in claim 32.

7. Claims 8-11,16-21,29,30, and 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Swanstrom, U.S. Pat. No. 5,822,568.

As per claim 8, Swanstrom shows a method of processing interrupts, the method comprising: detecting interrupt signals; determining if the interrupt signals are from local devices or expansion devices; directing a direct memory access controller to read a status register for any expansion devices that have generated interrupt signals; processing any interrupt signals from local devices; and processing any interrupt signals from devices located across the bus (abstract, figs. 12,14,16 and throughout cols. 9-13, wherein the DMAC detects the interrupt

signals and depending on the CPU–set start condition the DMAC handles the interrupt and/or passes an interrupt to the CPU). Swanstrom shows all of the elements recited in claim 8.

As for claim 9, the argument for claim 8 applies. Swanstrom also shows detecting interrupt signals further comprising receiving interrupt signals at a central processor (abstract, figs. 12,14,16 and throughout cols. 9-13). Swanstrom shows all of the elements recited in claim 9.

As for claim 10, the argument for claim 8 applies. Swanstrom also shows determining further comprising determining that the interrupt signals are from local devices and any expansion devices further comprise no expansion devices (abstract, figs. 12,14,16 and throughout cols. 9-13). Swanstrom shows all of the elements recited in claim 10.

As for claim 11, the argument for claim 8 applies. Swanstrom also shows determining further comprising determining that the interrupt signals are from expansion devices and directing a memory access controller further comprises directing a memory access controller to process a second interrupt while processing a first interrupt (abstract, figs. 12,14,16 and throughout cols. 9-13). Swanstrom shows all of the elements recited in claim 11.

As per claim 16, Swanstrom shows a method of processing interrupts, the method comprising: detecting an interrupt at a direct memory access controller from a device located across a bus from a central processor; transferring data from the device to a local memory; and generating an interrupt signal to central processor when transfer is complete (abstract and figs. 12,14,16). Swanstrom shows all of the elements recited in claim 16.

As for claim 17, the argument for claim 16 applies. Swanstrom also shows detecting an interrupt further comprising receiving an interrupt on an interrupt line to a direct memory access controller (cols. 9-13). Swanstrom shows all of the elements recited in claim 17.

As for claim 18, the argument for claim 16 applies. Swanstrom also shows detecting an interrupt further comprising using a direct memory access controller to detect a voltage change on an interrupt line (cols. 9-13, and inherent in that all signals are detected in modern electronic devices by detecting voltages on the lines). Swanstrom shows all of the elements recited in claim 18.

As per claim 19, Swanstrom shows a device, comprising: a central processor (fig.7,(710)) having at least one direct memory access controller (750); an expansion bus (730 or 794); at least one expansion device in communication with the central processor through the expansion bus (740); and at least one interrupt signal line electrically coupled between the direct memory access controller and the expansion bus (742). Swanstrom shows all of the elements recited in claim 19.

As for claim 20, the argument for claim 19 applies. Swanstrom also shows at least one interrupt signal line further comprising at least one interrupt signal line directly connected to the direct memory access controller (742). Swanstrom shows all of the elements recited in claim 20.

As for claim 21, the argument for claim 19 applies. Swanstrom also shows at least one interrupt signal line further comprising a detection line electrically coupled between a central interrupt signal line and a direct memory access controller (abstract, figs. 7,12,14,16 and throughout cols. 9-13). Swanstrom shows all of the elements recited in claim 21.

As per claim 29, Swanstrom shows an article of machine-readable media, the article containing instructions that when executed cause the machine to; detect interrupt signals; determine if the interrupt signals are from local devices or expansion devices; direct a direct memory access controller to read a status register for any expansion devices that have generated interrupt signals; process any interrupt signals from local devices; and process any

interrupt signals from devices located across the bus (abstract, figs. 7,12,14,16 and throughout cols. 9-13). Swanstrom shows all of the elements recited in claim 29.

As per claim 30, Swanstrom shows a device, comprising: means for detecting interrupt signals; means for determining sources of the interrupt signals; means for directing a direct memory access controller to read a status register for any expansion devices that have generated interrupt signals; means for processing any interrupt signals from local devices; and processing any interrupt signals from expansion devices (abstract, figs. 7,12,14,16 and throughout cols. 9-13). Swanstrom shows all of the elements recited in claim 30.

As per claim 33, Swanstrom shows a device, comprising: means for detecting an interrupt at a direct memory access controller from an expansion device; means for transferring data from the device to a local memory; and means generating an interrupt signal to central processor when transfer is complete (abstract, figs. 7,12,14,16 and throughout cols. 9-13). Swanstrom shows all of the elements recited in claim 33.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 3-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams in view of Swanstrom.

As for claim 3, the argument for claim 1 applies. Williams does not specifically show detecting an indicator of an interrupt further comprising receiving an interrupt on an interrupt line to a direct memory access controller. However, as noted above, Swanstrom shows detecting

interrupts on an interrupt line coupled to a DMA controller (abstract and fig.7). It would have been obvious to one of ordinary skill in the art to use a DMA controller to receive interrupts as shown by Swanstrom in the system on Williams in order to allow the CPU to be more responsive to real-time events (see the abstract of Swanstrom).

As for claim 4, the argument for claim 1 applies. Williams does not specifically show detecting an indicator of an interrupt further comprising using a direct memory access controller to detect a voltage change on an interrupt line. However, as noted above, Swanstrom shows detecting interrupts on an interrupt line coupled to a DMA controller (abstract and fig.7). It would have been obvious to one of ordinary skill in the art to use a DMA controller to receive interrupts as shown by Swanstrom in the system on Williams in order to allow the CPU to be more responsive to real-time events (see the abstract of Swanstrom).

As for claim 5, the argument for claim 1 applies. Williams does not specifically show transferring data further comprising using a direct memory access controller to transfer data from any expansion devices that generated interrupt signals. However, as noted above, Swanstrom shows detecting interrupts on an interrupt line coupled to a DMA controller (abstract and fig:7). It would have been obvious to one of ordinary skill in the art to use a DMA controller to receive interrupts as shown by Swanstrom in the system on Williams in order to allow the CPU to be more responsive to real-time events (see the abstract of Swanstrom).

As for claim 6, the argument for claim 1 applies. Williams does not specifically show transferring data further comprising using a direct memory access controller to transfer data from expansion device to local memory and generating an interrupt to a central processor. However, as noted above, Swanstrom shows detecting interrupts on an interrupt line coupled to a DMA controller (abstract and fig.7). It would have been obvious to one of ordinary skill in the art to use a DMA controller to receive interrupts as shown by Swanstrom in the system on

Williams in order to allow the CPU to be more responsive to real-time events (see the abstract of Swanstrom).

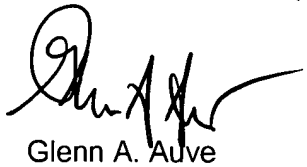
Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The other cited references show interrupt processing.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn A. Auve whose telephone number is (571) 272-3623. The examiner can normally be reached on M-F 8:00 AM-5:30 PM, every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Glenn A. Auve
Primary Examiner
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gaa
2 September 2005